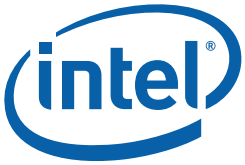

Implementing Industry Standard Architecture (ISA) with Intel® Express Chipsets

White Paper

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1 Introduction

ISA is still a commonplace technology in embedded systems, despite being an obsolete expansion bus technology in the sphere of personal computing. Due to the long lifetimes of embedded systems and the need to re-use existing system peripherals, it is often attractive for system designers to retain ISA compatibility in their system, despite the availability of newer and more advanced expansion bus technology.

The purpose of this document is to highlight any limitations in implementing an ISA expansion bus on a modern Intel® Express Chipset that a system designer may face.

1.1 Terminology

The following terminology applies for this document:

Term	Description
DMA	Direct Memory Access
ICH	I/O Controller Hub
I/O	Input/Output
ISA	Industry Standard Architecture
LPC	Low Pin Count
PCI	Peripheral Component Interconnect
PnP	Plug and Play

Note: *Intel® Express Chipset* refers to any chipset that includes an Intel® I/O Controller Hub 6, 7, 8, or 9 (ICH6, ICH7, ICH8 and ICH9)

1.2 Reference Documents

Document	Document No./Location
Intel® I/O Controller Hub 6 (ICH6) Family Datasheet	http://www.intel.com/design/chipsets/datashts/301473.htm
Intel® I/O Controller Hub 6 (ICH6) Family Specification Update	http://www.intel.com/design/chipsets/specupdt/301474.htm
Intel® I/O Controller Hub 7 (ICH7) Family Datasheet	http://www.intel.com/design/chipsets/datashts/307013.htm
Intel® I/O Controller Hub 7 (ICH7) Family Specification Update	http://www.intel.com/design/chipsets/specupdt/307014.htm
Intel® I/O Controller Hub 8 (ICH8) Family Datasheet	http://www.intel.com/design/chipsets/datashts/313056.htm
Intel® I/O Controller Hub 8 (ICH8) Family Specification Update	http://www.intel.com/design/chipsets/specupdt/313057.htm
Intel® I/O Controller Hub 9 (ICH9) Family Datasheet	http://www.intel.com/design/chipsets/datashts/316972.htm
Intel® I/O Controller Hub 9 (ICH9) Family Specification Update	http://www.intel.com/design/chipsets/specupdt/316973.htm

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2 ISA Bridge Support and Limitations

This chapter summarizes the two methods available to system designers for implementing an ISA bus in their design. It also describes the limitations that system designers will face in the implementation of each method. In both cases, system designers should work with the ISA bridge vendor to fully understand the impact on their design.

A list of vendors who provide bridges for each method is also provided. These lists are provided as a reference only and do not constitute a guarantee of operability with the Intel® Express Chipsets.

2.1 PCI / ISA Bridge

PCI to ISA bridge is the most common method of interfacing ISA devices to modern chipsets. In most respects, these devices perform like a standard PCI device. As such, it is a relatively simple for system designers to use such a bridge in their design. However, there are limitations in the PCI interface of Intel® Express chipsets that could limit the usefulness of a PCI to ISA bridge in the system's application. System designers should be aware of these limitations before proceeding with their design.

2.1.1 ISA DMA

ISA DMA or Bus Master transactions are not supported through the standard PCI Bus Master functionality. Instead, PCI/ISA bridges will implement the PC/PCI DMA and/or Distributed DMA specification to fulfill these transactions. As a result, it is necessary for the PCI controller to implement support for at least one of these specifications to facilitate ISA DMA or Bus Master support.

2.1.1.1 Distributed DMA

Distributed DMA is not supported in any of Intel's I/O Controller Hub variants.

2.1.1.2 PC/PCI DMA

The PC/PCI DMA protocol is supported on all I/O Controller Hubs from ICH to ICH5 (excluding 6300ESB). These parts have dedicated Request and Grant signals – REQ[A:B] and GNT[A:B] – to implement the hardware aspect of the protocol.

From ICH6 onwards these signals have been removed and, therefore, these devices no longer support the PC/PCI protocol. As a result, it is no longer possible to support ISA DMA or Bus Master transactions using a PCI/ISA bridge. A system designer should be aware of this limitation before using such a bridge.

If a system designer does not require ISA DMA or Bus Master functionality then it may still be possible to use the PCI/ISA bridge without the presence of the PC/PCI Request and Grant signals. It is recommended that a system designer works with the bridge vendor to understand if this approach is feasible.

2.1.2 Vendors

A list of PCI/ISA bridge vendors are included below.

- Winbond*
- National Semiconductor*
- ITE Tech Inc.*
- Interconnect Systems Solution (ISS)*

2.2 LPC / ISA Bridge

The Low Pin Count (LPC) bus offers a second method of connecting an ISA bridge to an ICH. LPC can be seen, in some ways, as a successor to ISA since it offers a way to connect low bandwidth and legacy peripherals to the system. Although LPC has substantially fewer signals than ISA it exceeds the bandwidth due to the fast bus speed and modern protocol. There are limitations, however, in the LPC interface of Intel® Express chipsets that could limit the usefulness of a LPC to ISA bridge in the system's application. System designers should be aware of these limitations before proceeding with their design.

2.2.1 Memory Transactions

The ISA protocol allows for memory-mapped transactions to components placed on the bus. In order to support these transactions it is, therefore, necessary to support memory-mapped transaction on the LPC bus.

The LPC specification specifies that such transactions are supported on the LPC bus. Indeed, on all I/O Controller Hubs up to and including ICH5 support these transactions. From ICH6 onwards, however, support for these transactions has been removed. As a result, it is not possible to support ISA memory mapped transactions on an Intel® Express chipset.

2.2.2 Other Limitations

Depending on the LPC/ISA bridge used, there may also be other limitations.

- Support for ISA bus mastering
- Support for certain 16-bit transactions

It is recommended that a system designer work with the LPC/ISA bridge vendor to understand the limitations.

2.2.3 Vendors

- Finktek*
- Winbond*

3 Architectural Limitations

This chapter describes some of the general architectural limitations which system designers should be aware of. A system designer should be aware of these limitations in order to properly plan for and allocate system resources.

3.1 I/O Aliasing

ISA devices are typically only capable of decoding 10-bit addresses for I/O cycles. The host bus (LPC or PCI), however, has a wider address space. For the ISA device, the additional address bits are a 'Don't Care' since it has no knowledge of them. As a result, the ISA device does not have a unique address for I/O cycles going to/from the host bus. Any address, whose first 10 bits match the ISA devices address, will be claimed by the ISA device irrespective of the remaining address bits.

Figure 1. I/O Address Aliasing

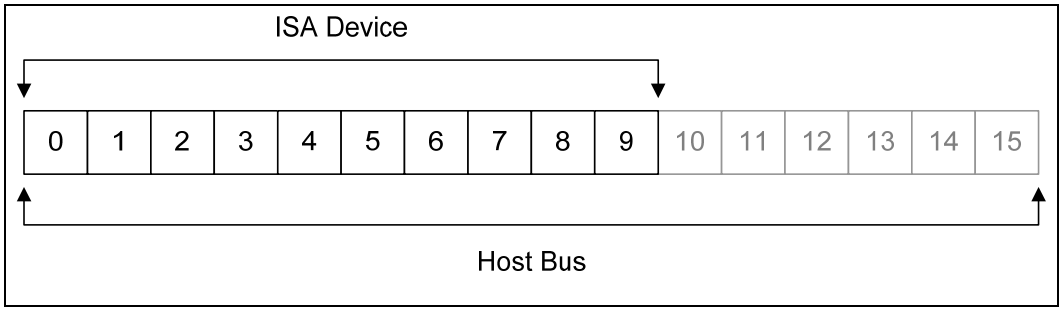

Figure 1 illustrates the problem of aliasing on a host bus with 16-bit addressing. 15:10 are the additional address bits that are a 'Don't Care' for the ISA device. The only way to guarantee that cycles meant for other devices are not claimed by the ISA device is to reserve all the possible addresses – where 9:0 is fixed and 15:10 can be from 000000b to 111111b. This is a very inefficient use of system resources and could have a knock-on effect to other system devices.

Note: For PCI/ISA bridges it is possible to configure the I/O Controller Hub to automatically compensate for I/O aliasing. This is done by setting the ISA Enable (IE) bit in BCRTL-Bridge Control Register (Device 30, Function 0, Offset: 3Eh-3Fh, Bit 2)

3.2 Plug and Play

The nature of the ISA bus architecture means that it is largely incapable of true Plug and Play (PnP). This limitation is in contrast with modern expansion bus technologies such as PCI and PCI Express* which were designed to be PnP from their inception.

The key points of PnP are the ability of the operating system to recognize all the devices on an expansion bus and know how to properly manage them & their associated system resources. In the case of ISA, there is no way for a modern operating system to detect the presence of connected devices. Neither is it possible for system resources to be dynamically assigned or de-assigned to those devices since the resource requirements are hard-wired. As a result, it is necessary to suitably configure the operating system – partly through direct configuration and partly through BIOS interaction - so it is aware of the system resources assigned to the device and does not try to allocate them to another device in the system.

Note: Some older operating systems, such as Windows* 98 and earlier, implemented memory and I/O range scans to discover typical ISA devices. A device discovered in this way would not, as a result, need to be reported by the BIOS. Most modern operating systems do not implement this feature and it is, therefore, necessary for the BIOS to report all ISA devices in the system. This makes it problematic to support ISA slots in an Intel® Express chipset system since, unless card usage is restricted to a known list, it is not possible to configure the BIOS to report all possible card types.

Later developments on ISA lead to an ISA PnP standard but this implementation only partially matches the full PnP feature set of modern expansion buses. Additionally, the ISA hardware needs to be designed to be PnP compatible. Older ISA hardware, not designed to the PnP specification would not be able to take advantage of this functionality.

4 Summary

Due to changes in architecture introduced in Intel® Express Chipsets, it is no longer possible to fully implement ISA in platforms based upon these chipsets. System designers may still use PCI/ISA or LPC/ISA bridges to add ISA support to their systems but they must be aware of the limitations applicable to either option.